IN THE SPECIFICATION

Please replace the Abstract with the following replacement Abstract:

Data-processing systems including processor datapaths that efficiently support computationally advantageous routing operations are disclosed. Data-processing methods based on such systems are also disclosed. [[A]] An exemplary data-processing system ~~comprises~~ includes a register file, a routing unit, a Banyan switch, ~~a switch control unit, a constant generator,~~ and an arithmetic logic unit. The arithmetic logic unit ~~comprises~~ may include a bitwise function unit, pipeline register, and an accumulator. The Banyan switch may have ~~an internal bitwidth of w and comprise~~ N data inputs and $\log_M(N)$ switching stages. [[N]] M may equal ~~$\log_2(w)$ or $\log_4(w)$~~ 2 or 4. In the case of ~~$\log_2(w)$~~ $\log_2(N)$ stages, each switching stage has N/2 switching cells. The routing unit ~~comprises~~ may include a control logic that generates a control signal, and various logics that respectively operate on various bit groups of the control signal. ~~The switch control unit comprises a shift constants generator, a pipeline flip-flop, and a switch tree. A data-processing method implemented by the above system is also disclosed.~~

Please replace the paragraph beginning on page 6, line 4, with the following replacement paragraph:

~~Figure 6B is~~ Figures 6B-1 and 6B-2 are a table that shows data of various output bits of the routing unit.

Please replace the paragraph beginning on page 6, line 14, with the following replacement paragraph:

~~Figure 8 is~~ Figures 8A-1 and 8A-2 are a block diagram of an embodiment for a Banyan switch.

Please replace Table 2C on page 18 with the following replacement Table 2C:

Bit Groups	Functions Control Bits	0	1	2	3	4	5	6	7
GROUP I	G1RG	0	0	0	0	1	0	1	0
	G1FG	0	0	0	1	0	0	0	0
	G1DG	1	0	0	0	0	0	0	0
	G1KG	0	0	0	0	0	1	0	0
GROUP IA	G1AFK	0	0	0	0	0	0	0	1
GROUP II	G2RG	0	0	0	1	1	0	1	0
	G2KG	0	0	0	0	0	1	0	0
	G2DG	1	0	0	0	0	0	0	0
GROUP III	G3RG	0	0	0	1	1	0	1	0
	G3KG	0	0	0	0	0	1	0	0
	G3CG	0	0	1	0	0	0	0	0
	G3VG	0	1	0	0	0	0	0	0
	G3DG	1	0	0	0	0	0	0	0
GROUP IV	G4RG	0	0	0	1	1	0	1	0
	G4KG	0	0	0	0	0	1	0	0
	G4DG	1	0	0	0	0	0	0	0
	G4F1	0	0	1	0	0	0	0	0
GROUP V	~~G5RKS~~ G5RK5	0	0	0	0	0	1	0	0
	G5F0	0	1	0	0	0	0	0	1
	G5F1	0	0	1	0	0	0	0	0
	G5SX	0	0	0	0	1	0	0	0
GROUP VI	~~G6RKS~~ G6RK5	0	0	0	0	0	1	0	0
	G6F0	0	0	0	0	1	0	0	1
	G6F1	0	0	1	0	0	0	0	0

TABLE 2C

Please replace the paragraph beginning on page 18, line 3, with the following replacement paragraph:

Figure 7B is a block logic diagram for Group VI bits. The logic 710 comprises four circuitry units one of which is shown in Figure 7B. The four units have different inputs and outputs. The inputs for the first unit are K63, ~~G6RKS~~ G6RK5, and R63, and the output is KB63. The inputs for the second unit are K62, ~~G6RKS~~ G6RK5, and R62, and the output is KB62. The inputs for the third unit are K61, ~~G6RKS~~ G6RK5, and R61, and the output is KB61. The inputs for the fourth unit are K60, ~~G6RKS~~ G6RK5, and R60, and the output is KB60.

Please replace the paragraph beginning on page 18, line 10, with the following replacement paragraph:

Figure 7C is a block logic diagram for Group V bits. The logic 720 comprises the sub-logic 722 and the sub-logic 724. The sub-logic 724 comprises forty-four circuitry units one of which is shown in Figure 7B. The forty-four units have different inputs and outputs. For example, the inputs for the first unit are K59, ~~G5RKS~~ G5RK5, and R59, and the output is KB59. The inputs for the second unit are K58, ~~G5RKS~~ G5RK5, and R58, and the output is KB58. The inputs for the forty-fourth unit are K16, ~~G5RKS~~ G5RK5, and R16, and the output is KB16.

Please replace the paragraph beginning on page 19, line 15, with the following replacement paragraph:

Figure 7E is a block logic diagram for Group III bits. The logic 740 comprises sub-logic 742 and 744. The sub-logic 742 generates C3 through C0 as inputs to the sub-logic 744. The sub-logic

744 comprises four circuitry units, one of which is shown in Figure 7E. The four units have different inputs and outputs. The inputs for the first unit are G3DG, D9, G3VG, R7, G3CG, C3, G3KG, K9, G3RG, and R9, and the output is KB9. The inputs for the second unit are G3DG, D8, G3VG, R6, G3CG, C2, G3KG, K8, G3RG, and R8, and the output is KB8. ~~The inputs for the second unit are G3DG, D8, G3VG, R6, G3CG, C2, G3KG, K8, G3RG, and R8, and the output is KB8.~~ The inputs for the third unit are G3DG, D7, G3VG, R5, G3CG, C1, G3KG, K7, G3RG, and R7, and the output is KB7. The inputs for the ~~second~~ fourth unit are G3DG, D6, G3VG, R4, G3CG, C0, G3KG, K6, G3RG, and R6, and the output is KB6.

Please replace the paragraph beginning on page 20, line 8, with the following replacement paragraph:

Figure 7G is a block logic diagram for Group IA bits. The inputs for the logic 760 are G1DG, D2, G1FG, F2, G1KG, K2, G1RG, and R2, and its output is KB2. Figure 7H is a block logic diagram for Group I bits. The logic ~~760~~ 770 comprises three circuitry units, one of which is shown in Figure 7H. The three units have different inputs and outputs. The inputs for the first unit are G1DG, D3, G1FG, F3, G1KG, K3, G1RG, and R3, and the output is KB3. The inputs for the second unit are G1DG, D1, G1FG, F1, G1KG, K1, G1RG, and R1, and the output is KB1. The inputs for the third unit are G1DG, D0, G1FG, F0, G1KG, K0, G1RG, and R0, and the output is KB0.